IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) A memory device, comprising:

a first variable resistor connected between a first terminal and a third terminal having a resistance which changes in accordance with a polarity of a pulse voltage between the first terminal and the third terminal; and

a second variable resistor connected between the third terminal and a second terminal having a resistance which changes in a direction opposite to a direction of change of the first variable resistor in accordance with a polarity of a pulse voltage between the third terminal and the second terminal.

2. (Original) The memory device according to claim 1, wherein the resistance value of the first variable resistor and the resistance value of the second variable resistor change in accordance with a first potential applied to two of the first terminal, the second terminal and the third terminal and a second potential different from the first potential applied to the other terminal of the first terminal, the second terminal and the third terminal.

3. (Original) The memory device according to claim 2, wherein the first potential is applied with a first pulse voltage at a first time to the two of the first terminal, the second terminal and the third terminal and the second potential is applied with a second pulse voltage at

the first time to the other terminal of the first terminal, the second terminal and the third terminal.

4. (Original) The memory device according to claim 3, wherein, at a second time, a third pulse voltage at the second potential is applied to the two of the first terminal, the second terminal and the third terminal and a fourth pulse voltage at the first potential is applied to the other terminal of the first terminal, the second terminal and the third terminal.

5. (Original) The memory device of claim 1, wherein resistance value of one of the first variable resistor and the second variable resistor is initialized to a value greater than that of the other variable resistor of the first variable resistor and the second variable resistor.

6. (Original) The memory device of claim 1, wherein

the polarity of the pulse voltage applied between the first terminal and the third terminal causes a resistance value of the first variable resistor to increase if the first terminal has a first polarity and to decrease if the first terminal has a second polarity opposite to the first polarity, and

the polarity of the pulse voltage applied between the third terminal and the second terminal causes a resistance value of the second variable resistor to increase if the third terminal has the first polarity and to decrease if the third terminal has the second polarity.

7. (Original) The memory device of claim 1, wherein a pulse voltage having a second potential is applied to the third terminal with the first and second terminals set at a first potential.

8. (Original) The memory device of claim 7, wherein the first potential is a ground potential, and the second potential is a potential other than the ground potential.

9. (Original) The memory device of claim 7, wherein the first potential is a positive potential or a negative potential and the second potential is the negative potential or the positive potential, respectively.

10. (Currently Amended) The memory device of claim 1, wherein at a first time ~~the~~ a first pulse voltage of the first polarity is applied to the first terminal and the third terminal and ~~the~~ a second pulse voltage of polarity opposite to the first polarity is applied to the second terminal, and at a second time the second pulse voltage is applied to the third terminal and the second terminal and the first pulse voltage is applied to the first terminal.

11. (Original) The memory device of claim 1, wherein a voltage at the third terminal is output with a first potential applied to the first terminal and a second potential applied to the second terminal.

12. (Original) A memory device whose resistance value changes in accordance with a pulse voltage applied thereto, the device comprising:

a plurality of memory cells, each memory cell comprising:

a transistor formed on a semiconductor substrate and having a source, a drain and a gate;

an insulating layer formed over the transistor;

a variable resistance layer formed over the insulating layer; and

two electrodes formed on the variable resistance layer,

wherein at least one of the drain and the source of the transistor are electrically connected to the two electrodes.

13. (Original) The memory device according to claim 12, wherein each memory cell further comprises:

a conductive layer formed on the insulating layer; and

a contact plug electrically connecting the at least one of the drain and the source of the transistor to the conductive layer.

14. (Original) The memory device of claim 12, wherein the variable resistance layer is an oxide with a perovskite structure.

15. (Original) The memory device of claim 14, wherein the oxide with the perovskite structure is a giant magnetoresistance material.

16. (Original) The memory device of claim 14, wherein the oxide with the perovskite structure is a high temperature superconducting material.

17. (Original) The memory device of claim 12, wherein the variable resistance layer is an oxide with an ilmenite structure.

18. (Original) The memory device of claim 17, wherein the oxide with the ilmenite structure is a nonlinear optical material.

19. (Original) The memory device of claim 13, wherein the conductive layer is made of one or more materials selected from the group consisting of Pt, Ag, Au, Ir, Ru, Ti, Ta, Al, Cu, RuO_3, RuO_2, $SrRuO_3$, $LaCoO_3$, $SrCoO_3$, $LaSrCoO_3$, TiN, TiO_x, $YBa_2Cu_3O_x$, IrO_2, TaSiN and MoN.

20. (Original) The memory device of claim 12, wherein each of the two electrodes is made of one or more materials selected from the group consisting of Cu, Al, Ag, Pt, Au, Ir, Ru, Os, Ti and Ta.

21. (Original) A memory circuit, comprising:

a first memory block connected between a first node and a second node;

a first block-selecting transistor connected in series with the first memory block between the first node and the second node; and

a second memory block connected between an interconnect node and a third node, the interconnect node connecting the first memory block and the first block-selecting transistor to each other,

wherein each of the first and second memory blocks includes a plurality of memory cells connected in series, and

each of the plurality of memory cells includes

a variable resistor connected between a first terminal and a second

terminal and whose resistance value changes in response to a pulse voltage applied between the first terminal and the second terminal, and

a transistor connected in parallel with the variable resistor between the first terminal and the second terminal.

22. (Original) The memory circuit of claim 21, wherein during writing of data,

the first block-selecting transistor is turned ON,

a transistor in a first memory cell of each of the plurality of the memory cells of the first memory block is turned OFF and a transistor in each memory cell other than the first memory cell of the plurality of memory cells in the first memory block is turned ON, and

a transistor in a second memory cell of each of the plurality of memory cells of the second memory block is turned OFF and a transistor in each memory cell other than the second memory cell of the plurality of memory cells in the second memory block is turned ON.

23. (Original) The memory circuit according to claim 22, wherein during writing of data, a pulse voltage for increasing a resistance value of a variable resistor included in the first memory cell is applied between the first node and the second node, and a pulse voltage for reducing the resistance value of a variable resistor included in the second memory cell is applied between the first node and the third node.

24. (Original) The memory circuit of claim 21, wherein during reading of data,

the first block-selecting transistor is turned ON,

a transistor in a first memory cell of the plurality of the memory cells of the first memory block is turned OFF and a transistor in each memory cell other than the first memory cell of the

plurality of memory cells in the first memory block is turned ON, and

a transistor in a second memory cell of the plurality of memory cells of the second memory block is turned OFF and a transistor included in each memory cell other than the second memory cell of the plurality of memory cells in the second memory block is turned ON.

25. (Original) The memory circuit according to claim 24, wherein a voltage at the first node is detected with a given voltage applied between the second node and the third node.

26. (Original) The memory circuit according to claim 21, wherein each of the plurality of memory cells are arranged in a matrix.

27. (Currently Amended) A memory circuit, comprising:

a first memory block connected between a ~~first~~ node ~~and a second node~~ receiving a variable power supply and a first bit line;

a first block-selecting transistor connected in series with the first memory block between the first bit line and the ~~second~~ node;

a second memory block connected between the ~~second~~ node ~~and a third node~~ receiving the variable power supply and a second bit line different from the first bit line; and

a second block-selecting transistor connected in series with the second memory block between the second ~~node~~ bit line and the ~~third~~ node,

wherein each of the first and second memory blocks includes a plurality of memory cells connected in series, and

each of the plurality of memory cells includes

a variable resistor connected between a first terminal and a second terminal and whose resistance value changes in response to a pulse voltage applied between the first terminal and the second terminal, and

a transistor connected in parallel with the variable resistor between the first terminal and the second terminal.

28. (Original) The memory circuit of claim 27, wherein during writing of data,

the first block-selecting transistor and the second block-selecting transistor are turned ON,

a transistor in first a memory cell of the plurality of memory cells in the first memory block is turned OFF and a transistor in each memory cell other than the first memory cell of the plurality of memory cells in the first memory block is turned ON, and

a transistor in a second memory cell of the plurality of memory cells in the second memory block is turned OFF and a transistor in each memory cell other than the second memory cell of the plurality of memory cells in the second memory block is turned ON.

29. (Original) The memory circuit of claim 28, wherein during writing of data, a pulse voltage for increasing the resistance value of a variable resistor included in the first memory cell is applied between the first node and the second node, and a pulse voltage for reducing the resistance value of a variable resistor included in the second memory cell is applied between the second node and the third node.

30. (Original) The memory circuit of claim 27, wherein during reading of data,

the first block-selecting transistor and the second block-selecting transistor are turned ON,

a transistor in a first memory cell of the plurality of memory cells in the first memory circuit is turned OFF and a transistor included in each memory cell other than the first memory cell of the plurality of memory cells in the first memory block is turned ON, and

a transistor in a second memory cell of the plurality of memory cells in the second memory circuit is turned OFF and a transistor in each memory cell of the plurality of memory cells other than the second memory cell is turned ON.

31. (Original) The memory circuit of claim 30, wherein during reading of data, a voltage at the second node is detected with a given voltage applied between the first node and the third node.

32. (Currently Amended) A method for writing of data in a variable resistance memory cell having at least three terminals and for resetting the variable resistance memory cell, comprising the steps of:

applying a first potential to two terminals of the at least three terminals of the variable resistance memory cell;

applying a second potential to a terminal other than the two terminals of the variable resistance memory cell[[.]] ;

changing a resistance value of a first variable resistance device of the variable resistance memory cell; and

changing a resistance value of a second variable resistance device of the variable

resistance memory cell in a direction opposite to that of the first variable resistance memory device.

33. (Original) The method of claim 32, wherein during data writing, the second potential has a first polarity and during a resetting operation, the second potential has a second polarity opposite of the first polarity.

34. (Original) The method of claim 32, further comprising the steps of:

changing a resistance value of a first variable resistance device of the variable resistance memory cell;

changing a resistance value of a second variable resistance device of the variable resistance memory cell in a direction opposite to that of the first variable resistance memory device.

35. (Original) The method of claim 32, wherein

the step of applying the first potential comprises applying a first pulse of the first potential at a first time, and

the step of applying the second potential comprises applying a second pulse of the second potential at the first time having a second polarity opposite of a first polarity of the first pulse.

36. (Original) The method of claim 35, further comprising the steps of:

applying a third potential of the second polarity to two terminals of the at least three terminals of the variable resistance memory cell at a second time; and

applying a fourth potential of the first polarity to a terminal other than the two terminals of the variable resistance memory cell at the second time.

37. (Currently Amended) A method for reading of data in a variable resistance memory cell having at least three terminals, comprising the steps of:

providing the variable resistance memory cell having a common access transistor connected in series to an output node and a first variable resistance device and a second variable resistance device connected in parallel to the output node;

applying a ground voltage to a ~~first~~ terminal ~~of at least three terminals~~ the first variable resistance device;

applying a reproducing voltage that is lower ~~that~~ than a recording voltage to a ~~second~~ terminal of the ~~at least three terminals~~ second variable resistance device;

outputting a voltage from ~~a third terminal of the at least three terminals~~ the output terminal.

38. (Original) The method for reading of data according to claim 37, wherein the voltage output has multiple values corresponding to a number of voltage pulses applied in a recording operation.

39. (Currently Amended) A memory cell for storing at least one bit of data, comprising:

first variable resistance means for changing resistance in accordance with a polarity of a pulse voltage between a first terminal and a third terminal; and

second variable resistance means for changing resistance in a direction opposite to a

direction of change of the first variable resistance means in accordance with a polarity of a pulse voltage between ~~a~~ the third terminal and ~~the~~ a second terminal.